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Original Article

Designing Resilient SRAM Architectures Against Soft Errors And Multi-Node Upsets For Aerospace Applications

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Abstract

This paper presents a radiation-tolerant Quad-node 10-transistor (10T) SRAM cell designed to achieve enhanced soft error robustness while maintaining low power consumption, high reliability, and stable noise margins. Conventional SRAM design metrics primarily focus on Read Static Noise Margin (RSNM), power efficiency, and reliability; however, radiation-tolerant SRAM cells additionally require strong immunity against soft errors caused by radiation-induced disturbances. In the proposed design, the NMOS access transistors used in the conventional Quatro 10T SRAM cell are replaced with PMOS access transistors to improve radiation tolerance. The use of PMOS access transistors significantly reduces radiation-induced leakage current variations, as PMOS devices are less sensitive to radiation bombardment compared to NMOS devices. During hold operation, both the conventional Quatro and the proposed 10T SRAM cells exhibit identical power consumption because the access transistors remain in cutoff mode. Furthermore, the proposed cell benefits from lower gate leakage currents due to the PMOS access structure. Both SRAM cells successfully recover from 1→0 single event transients (SETs) during hold operation. For 0→1 SETs, the proposed SRAM cell demonstrates an improvement of 3 μA in current margin, thereby reducing hold failure probability and enhancing soft error resilience. This improvement is achieved with only a 2.04% increase in read access time, while other performance metrics, including RSNM, hold power, Write Static Noise Margin (WSNM), and cell area, remain unchanged.

Introduction

The rapid advancement of electronic gadgets and portable systems has significantly accelerated the growth of Very Large Scale Integration (VLSI) technology. Modern electronic systems such as smartphones, satellites, defense equipment, medical devices, radars, GPS systems, and communication networks heavily depend on semiconductor memories for storing and processing data. Among different memory technologies, Static Random Access Memory (SRAM) plays a crucial role because of its high-speed read and write operations, making it suitable for cache memories, register files, and System-on-Chip (SoC) applications. However, with continuous CMOS technology scaling and reduction in feature size, SRAM cells have become highly vulnerable to radiation-induced soft errors.

Radiation particles such as alpha particles, neutrons, protons, and heavy ions can strike sensitive regions of SRAM transistors, generating unwanted transient currents and voltage fluctuations. These disturbances can alter the stored data in memory cells, causing Single Event Transients (SETs) and Single Event Upsets (SEUs). Such soft errors are especially critical in aerospace, military, biomedical, and industrial applications where high reliability is essential. Conventional SRAM cells fail to provide sufficient robustness under radiation environments due to reduced supply voltage, lower node capacitance, and shrinking noise margins in nanoscale technologies.

To address these challenges, several radiation-hardened SRAM architectures such as DICE 12T, Quatro 10T, and other hardened SRAM cells have been proposed in literature. These designs aim to improve soft error tolerance while maintaining acceptable power consumption, area overhead, and operational stability. The proposed work focuses on the design of a Quad-node 10-transistor (10T) SRAM cell with improved radiation tolerance and reduced leakage current. In this design, conventional NMOS access transistors are replaced with PMOS access transistors because PMOS devices exhibit superior radiation tolerance and lower leakage current under radiation bombardment. The proposed SRAM cell improves soft error robustness, especially during 0→1 Single Event Transients, by increasing the current margin and reducing hold failure probability.

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The proposed SRAM cell maintains comparable Read Static Noise Margin (RSNM), Write Static Noise Margin (WSNM), hold power consumption, and cell area while providing enhanced reliability. Although a slight increase in read access time is observed, the overall improvement in radiation hardness and soft error tolerance makes the design highly suitable for modern low-power and space-oriented applications. Therefore, radiation-hardened SRAM cells are becoming increasingly important in ensuring reliable memory operation in advanced nanoscale VLSI systems.

Radiation Environments

The radiation environment significantly affects electronic devices and systems across several domains, including space, ground level, nuclear reactors, radiation processing industries, weapons systems, and high-energy physics experiments. In space, radiation consists mainly of radiation belts, cosmic rays, and solar flares. Radiation belts contain trapped charged particles such as electrons and protons, while cosmic rays originate from galactic, solar, and terrestrial sources. Solar flares release bursts of protons, electrons, and alpha particles during solar storms. These radiations can degrade electronic components through accumulated ionization or by single energetic particles striking sensitive circuit nodes, causing failures known as single-event effects. To reduce these impacts, space missions use radiation-hardened or radiation-tolerant electronics. At ground level, radiation effects were first observed in memory chips due to alpha particles from packaging materials. Cosmic rays also generate atmospheric neutrons that can upset semiconductor devices such as SRAMs and DRAMs. Although weaker than space radiation, these effects still influence the reliability of computer systems and industrial electronics. In nuclear reactor environments, the primary radiation sources are neutrons and gamma rays. Equipment within containment structures must withstand continuous exposure over long operational lifetimes and remain functional during accidents. Radiation effects are evaluated along with other stress factors to ensure safety and durability. Radiation processing uses controlled radiation for beneficial purposes. Applications include food preservation, sterilization of medical products, waste treatment, water purification, polymer modification, and semiconductor processing. Gamma sources and electron accelerators are commonly used in these industries. Nuclear weapons produce radiation through thermal energy, blast effects, nuclear radiation, and electromagnetic pulses. Radiation includes neutrons, gamma rays, and other particles that can damage electronics and materials. High-energy physics accelerators such as the CERN Large Hadron Collider create extremely hostile radiation environments with very high dose rates, requiring advanced radiation-resistant electronic systems.

Radiation Hardened by Design

Radiation-induced soft errors in SRAMs can be reduced using Radiation Hardened by Process (RHBP) and Radiation Hardened by Design (RHBD) techniques. RHBP modifies the manufacturing process, making it expensive, while RHBD is easier and widely preferred. Common RHBD methods include Error Correction Codes (ECC), which detect and correct bit errors, though they increase memory access time, and circuit duplication techniques like Triple Modular Redundancy (TMR), which improve reliability but consume more power and area. Radiation-hardened SRAM cells such as Dual Interlock Storage Cell (DICE) and Quatro cells provide strong resistance against single-event upsets (SEUs). DICE cells are highly reliable but occupy larger chip area, while Quatro cells offer better resilience in advanced technologies. Single-event effects occur when energetic particles strike CMOS devices, causing ionization and charge collection. These effects include soft upsets such as SEU, multiple-bit upset (MBU), and single-event functional interrupt (SEFI), which temporarily alter data or functionality. Hard upsets, including single-event latch-up (SEL), gate rupture (SEGR), and burn out (SEBO), may permanently damage devices.

Existing SRAM Bitcell Designs

The existing SRAM bitcell systems mainly include the conventional 6T SRAM cell, DICE cell, and Quatro 10T SRAM cell. These designs are widely used in memory systems to balance area, speed, stability, and radiation tolerance. The conventional 6T SRAM bitcell is the most commonly used structure in industry due to its compact size and simple design. It consists of two cross-coupled inverters and two access transistors. The cell stores data using two internal nodes, Q and QB. During read and write operations, bit lines and word lines control data access. The major advantage of the 6T cell is its small area and high performance. However, it is highly sensitive to radiation strikes and soft errors because flipping one internal node can easily disturb the entire stored data. To improve reliability, the Dual Interlocked Storage Cell (DICE) was introduced. DICE uses four storage nodes and interlocked inverters to provide redundancy.

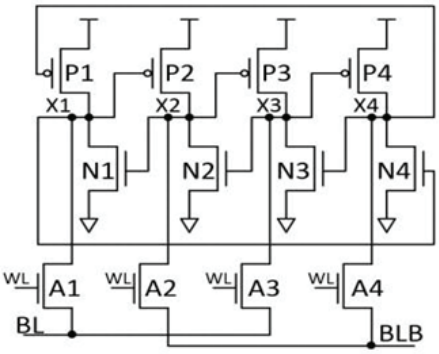

***Fig. 1**. Schematic of DICE Bit cell*

This structure can recover from single event upsets (SEUs), making it more robust than the 6T SRAM cell. However, in advanced nanoscale technologies, multiple nodes may be affected simultaneously, reducing its effectiveness. Another improved design is the Quatro 10T SRAM cell. It uses ten transistors and CVSL logic to reduce area overhead while still providing soft-error recovery capability. Compared to DICE, Quatro offers better area efficiency and improved radiation tolerance, although some nodes remain sensitive to SEU conditions.

Proposed Cell, Operations

The proposed system is a radiation-hardened 10-transistor (10T) SRAM cell designed to improve the reliability and robustness of memory circuits used in aerospace and nanoscale applications. Modern SRAM cells are highly vulnerable to radiation-induced soft errors because of reduced supply voltage, smaller node capacitance, and increased process variations in deep submicron technologies. High-energy particles such as alpha particles, cosmic rays, and neutrons can generate transient currents in sensitive storage nodes, resulting in Single Event Upsets (SEUs). These soft errors can disturb stored data and affect the overall performance of digital systems. To overcome

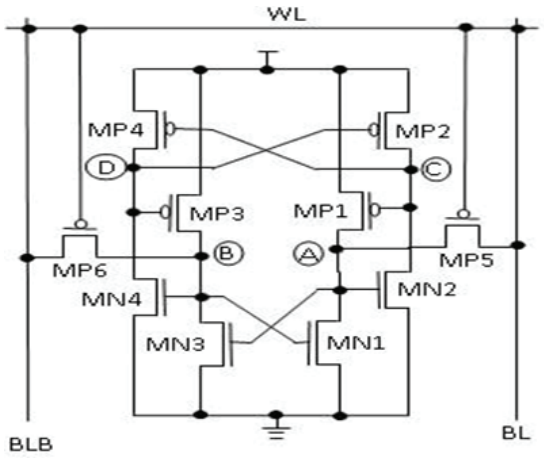

Figure: Schematic of proposed 10T SRAM cell with PMOS access transistors

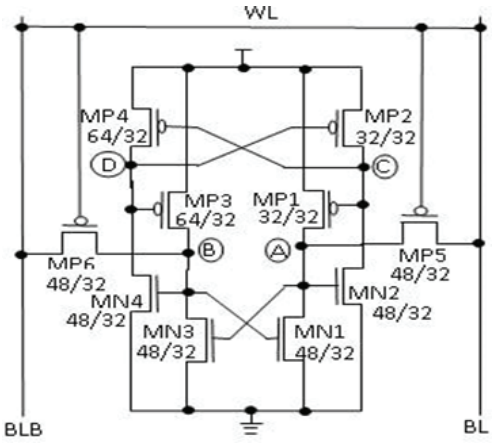

Figure: Cell Sizing of the proposed 10T SRAM cell (all the W/L dimensions of the MOSFETs are in nanometers)

these challenges, the proposed system introduces a modified 10T SRAM architecture using PMOS access transistors instead of conventional NMOS access transistors.

Architecture of the Proposed 10T SRAM Cell

The proposed SRAM cell consists of four PMOS transistors (MP1–MP4), four NMOS transistors (MN1–MN4), and two PMOS access transistors connected to bit lines BL and BLB. Similar to the Quatro-10T SRAM cell, the circuit operates using cross-coupled inverter pairs to store binary data. The main difference is the replacement of NMOS access transistors with PMOS access transistors to enhance radiation tolerance.

When a logic value is stored at one node, the complementary nodes maintain opposite values through feedback action. This cross-coupled arrangement ensures stable data retention even when transient disturbances occur. PMOS devices are selected because they exhibit lower leakage current under radiation exposure compared to NMOS devices. Additionally, PMOS transistors have lower gate leakage, which improves hold stability and minimizes data corruption during standby mode.

Cell Sizing and Stability

Proper transistor sizing is critical for achieving stable read and write operations. The proposed system maintains an optimized cell ratio to ensure high Read Static Noise Margin (RSNM) and improved write ability. The pull-down transistors are designed stronger than the access transistors to prevent accidental flipping during read operations. Similarly, PMOS pull-up transistors are sized appropriately to restore logic levels effectively after transient disturbances.

The proposed SRAM cell uses transistor dimensions similar to the Quatro-10T design, except for the PMOS access transistors. This sizing strategy helps the cell retain data even when affected by radiation-induced transient currents. The measured RSNM value is approximately 222 mV, while the Write Static Noise Margin (WSNM) is around 175 mV, indicating stable operation under noise conditions.

) Performance Analysis

The proposed system was evaluated using parameters such as Read Access Time (TRA), Hold Power, RSNM, WSNM, and Soft Error Robustness. Although the proposed cell shows slightly higher read delay due to the lower mobility of holes in PMOS transistors, the delay remains acceptable for reliable operation. Hold power remains nearly identical to the conventional Quatro-10T cell because the access transistors are turned OFF during standby mode.

The major improvement is observed in soft error robustness. The proposed SRAM cell withstands stronger radiation-induced transient currents before flipping occurs. The current margin improves from 229 µA in the Quatro-10T cell to 232 µA in the proposed design, demonstrating enhanced tolerance against Single Event Upsets.

Results

Read Access Time (TRA) is an important performance parameter in SRAM cells. It represents the time required for the bit line voltage difference to reach 50 mV after activation of the word line, enabling reliable sensing by the sense amplifier. The comparison of TRA values for the Quatro 10T SRAM cell and the proposed 10T SRAM cell at different supply voltages (VDD) is shown below.

Table: Comparison of TRA Values for Different VDD

VDD (Volts)	Quatro 10T SRAM (s)	Proposed 10T SRAM (s)
0.60	2.828×10^{-11}	2.804×10^{-11}
0.65	1.955×10^{-11}	1.995×10^{-11}
0.70	1.463×10^{-11}	1.526×10^{-11}
0.75	1.155×10^{-11}	1.224×10^{-11}
0.80	9.485×10^{-12}	1.017×10^{-11}

From the above comparison, it is observed that the Read Access Time decreases as the supply voltage (VDD) increases for both SRAM cells. Higher supply voltage improves transistor switching speed and increases current driving capability, resulting in faster read operations.

The Quatro 10T SRAM cell exhibits slightly lower TRA values compared to the proposed 10T SRAM cell at most supply voltages. This is because the Quatro cell uses NMOS access transistors, where electrons act as majority charge carriers. Electrons have higher mobility than holes, enabling faster charge transfer and reduced read delay.

In contrast, the proposed 10T SRAM cell uses PMOS access transistors to improve radiation hardness and reduce leakage

current under radiation exposure. Since holes are the majority carriers in PMOS devices and possess lower mobility than electrons, the proposed cell experiences slightly higher read access time. However, the increase in delay is minimal and remains within acceptable limits for reliable memory operation.

The proposed 10T SRAM cell sacrifices a small amount of speed in exchange for improved soft error robustness, better data retention, and enhanced radiation tolerance. Therefore, the proposed design is more suitable for aerospace and high-reliability applications where stability and radiation resistance are more critical than achieving the minimum read delay.

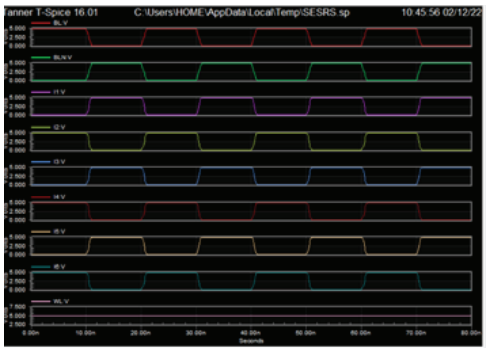

Figure: Existing Wave Forms

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Power Results

VV1 from time 0 to 0e+000
Average power consumed -> 1.225569e-004 watts
Max power 8.664466e-003 at time 2.04372e-009
Min power 0.000000e+000 at time 1.1e-008

VV2 from time 0 to 0e+000
Average power consumed -> 4.698539e-004 watts
Max power 1.537856e-002 at time 4.06072e-009
Min power 3.146716e-009 at time 6.875e-010

VV3 from time 0 to 0e+000
Average power consumed -> 3.414352e-005 watts
Max power 5.468436e-003 at time 3.03933e-009
Min power 0.000000e+000 at time 0
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Figure: Power For Existing System

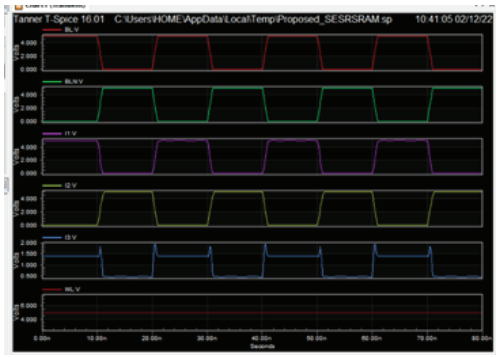

Figure: Proposed System Wave Forms

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Power Results

VV1 from time 0 to 8e-008
Average power consumed -> 3.417924e-003 watts
Max power 6.959062e-003 at time 2.1e-008
Min power 0.000000e+000 at time 1.1e-008

VV3 from time 0 to 8e-008
Average power consumed -> 3.577589e-005 watts
Max power 1.182511e-003 at time 1.05722e-008
Min power 0.000000e+000 at time 0

VV4 from time 0 to 8e-008
Average power consumed -> 8.425136e-007 watts
Max power 1.403366e-004 at time 4.0905e-008
Min power 0.000000e+000 at time 0
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Figure: Power Results for Proposed System

Conclusion

We have presented a 10T SRAM cell that uses PMOS access transistors, which is more soft error robust, compared to that of Quatro-10T cell at 22-nm technology. All the readings are taken with 5000 sample size while performing Monte Carlo simulation. The increment of 3µA in current margin implies that proposed cell withstands flipping to current spikes which are stronger which makes it reliable compared to Quatro-10T cell. The unaffected PMOS transistors leakage currents after radiation bombardment and hence usage of PMOS access transistors in proposed 10-T SRAM cell makes it more radiation hardened than Quatro-10T cell. The increment in current margin suggests the better application of the proposed cell in radiation environment or in aerospace industry. Therefore, the proposed cell remains as an attractive choice aerospace application.

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